**INSTITUTO POLITÉCNICO NACIONAL**

**ESCUELA SUPERIOR DE CÓMPUTO**

**------------------DISEÑO DE SISTEMAS DIGITALES---------------**

**TAREA 1**

Decodificadores

**ALUMNO:**

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**GRUPO:**

2CM14

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BCD A 7 SEGMENTOS CON ENTRADA DE CONTROL

Diagrama, Esquemático

Descripción generada automáticamenteTabla de verdad control igual a 0

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **#** | **C** | **E3** | **E2** | **E1** | **E0** | **A** | **B** | **C** | **D** | **E** | **F** | **G** |
| **0** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| **1** | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| **2** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| **3** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| **4** | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| **5** | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| **6** | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| **7** | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| **8** | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **9** | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| **A** | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **B** | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **C** | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **D** | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **E** | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **F** | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Tabla de verdad control igual a 1

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **#** | **C** | **E3** | **E2** | **E1** | **E0** | **A** | **B** | **C** | **D** | **E** | **F** | **G** |
| **0** | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| **1** | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| **2** | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| **3** | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| **4** | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| **5** | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| **6** | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| **7** | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| **8** | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **9** | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| **A** | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| **B** | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| **C** | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| **D** | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| **E** | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| **F** | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

Descripción en VHDL

library ieee;

use ieee.std\_logic\_1164.all;

entity DECO is

port( E: in std\_logic\_vector(3 downto 0);

C: in std\_logic;

DISPLAY: out std\_logic\_vector(6 downto);

);

end entity;

architecture A\_DECO of DECO is

constant DIG0: std\_logic\_vector(6 downto 0):=“0000001”;

constant DIG1: std\_logic\_vector(6 downto 0):=“1001111”;

constant DIG2: std\_logic\_vector(6 downto 0):=“0010010”;

constant DIG3: std\_logic\_vector(6 downto 0):=“0000110”;

constant DIG4: std\_logic\_vector(6 downto 0):=“1001100”;

constant DIG5: std\_logic\_vector(6 downto 0):=“0100100”;

constant DIG6: std\_logic\_vector(6 downto 0):=“1100000”;

constant DIG7: std\_logic\_vector(6 downto 0):=“0001111”;

constant DIG8: std\_logic\_vector(6 downto 0):=“0000000”;

constant DIG9: std\_logic\_vector(6 downto 0):=“0001100”;

constant DIGA: std\_logic\_vector(6 downto 0):=“0001000”;

constant DIGB: std\_logic\_vector(6 downto 0):=“1100000”;

constant DIGC: std\_logic\_vector(6 downto 0):=“0110001”;

constant DIGD: std\_logic\_vector(6 downto 0):=“1000010”;

constant DIGE: std\_logic\_vector(6 downto 0):=“0110000”;

constant DIGF: std\_logic\_vector(6 downto 0):=“0111000”;

constant ERR: std\_logic\_vector(6 downto 0):= “1111111”;

begin

process(E, C)

begin

if( C = ‘0’) then

case E is

when “0000” => DISPLAY <= DIG0;

when “0001” => DISPLAY <= DIG1;

when “0010” => DISPLAY <= DIG2;

when “0011” => DISPLAY <= DIG3;

when “0100” => DISPLAY <= DIG4;

when “0101” => DISPLAY <= DIG5;

when “0110” => DISPLAY <= DIG6;

when “0111” => DISPLAY <= DIG7;

when “1000” => DISPLAY <= DIG8;

when “1001” => DISPLAY <= DIG9;

when others => DISPLAY <= ERR;

end case;

elsif(c = ‘1’) then

case E is

when “0000” => DISPLAY <= DIG0;

when “0001” => DISPLAY <= DIG1;

when “0010” => DISPLAY <= DIG2;

when “0011” => DISPLAY <= DIG3;

when “0100” => DISPLAY <= DIG4;

when “0101” => DISPLAY <= DIG5;

when “0110” => DISPLAY <= DIG6;

when “0111” => DISPLAY <= DIG7;

when “1000” => DISPLAY <= DIG8;

when “1001” => DISPLAY <= DIG9;

when “1010” => DISPLAY <= DIGA;

when “1011” => DISPLAY <= DIGB;

when “1100” => DISPLAY <= DIGC;

when “1101” => DISPLAY <= DIGD;

when “1110” => DISPLAY <= DIGE;

when “1111” => DISPLAY <= DIGF;

when others => DISPLAY <= ERR;

end case;

else

DISPLAY <= ERR;

end if;

end process;

end A\_DECO;